Eng. Research Bull.
Faculty of Eng. & Tech.
Menoufia University
Vol. VI Part 1,1984

pp. 165 - 175

A DIGITAL TELEVISION LINE-STORE FOR DIGITAL SIGNAL PROCESSING USING STANDARD CIRCUITS

Ibrahim Zakaria Morsi, Ph.D.,
Faculty of Electronic Engineering, Menouf.

ABSTRACT

A line store for storing one television line is a useful means of testing. Such a device would be of great value in quick subjective assessment for one-dimensional image processing, such as contouring effects and selection of different coding techniques in bit-rate reduction problems.Another useful possible application is also pattern generation for television signal assessments and tests. Combining more than one line store, a considerable number of different basic patterns could be realized.

The principal advantage of the design proposed in this paper is that the line store is built using standard off-shelf memory chips and other digital integrated circuit controlling circuitry.This leads to the direct application of experience gained in normal design procedures and low-cost obtained devices.

I. INTRODUCTION

One of the most practical aids to investigating digital television signal processing is, undoubtedly, a television line-store.[1,2] With such an equipment, a whole line of television signal can be stored and displayed on an ordinary monitor. This enables the experimenter to subjectively assess any processing scheme under test quickly,in order to get an over-look which may, or may not, justify any further and deeper investigations in the matter.

Pattern generation is another area where line-store could be of great help. For generation of different patterns, more than one line-store should be available. Ultimately,several hundreds of such a line-store would comprise a television frame-store,a device of great importance in assessing a whole image of any category.

The line-store consists mainly of two distinct parts. The first part is the analogue-to-digital and digital-to-analogue conversion, while the second part contains the memory and logic control circuits. For analogue and digital conversion, the matter is, in principles, the same as in ordinary conversion, except for the high speed associated with video signals, and which is achievable by using special high frequency circuits. As for the memory and control part, this will be considered now in detail.

II. SAMPLING FREQUENCY/MEMORY SPEED

As known, a television line period is about 64 usecond. A reasonable sampling rate, to be compatible with the chrominance subcarrier for colour signals will be in excess of 850 samples/line. For simplicity of operation, and with digital and binary circuits in mind, a number of 1024 (2^{10}), is a better choice in this design.

Thinking of memory circuits to cope with the fast sampling rate of video signals would require memory chips of access time in the range of several tens of nanoseconds (64 us/1024 = 62.5 ns). Such speed is , (at present), achievable only(in commercial economical availability)with limited technologies,such as Bipolar and Emitter-Coupled Logic (ECL).[3,4] In addition to the relatively high cost of such products, several

precautions should also be taken to account for the environmental noise due to the high switching speeds at such frequencies.

Standard MOS technology memory chips are low cost, but are of low speed, (longer access time) compared with video signals sampling rates.Multiplexing enables the use of MOS technology memory, to construct such a line-store.

A vector of data of size N digitized samples (words) is written (stored) in N memory locations. These memory locations are not consecutive in the same chip, but are rather distributed (multiplexed) among different Banks. Each word in the vector is stored in one of the banks, in sequence, and alternatively, as explained below.

Figure (1) shows a block diagram for the line-store design.The whole necessary memory area is divided into N banks, (modules), where N is a function of the multiplexing requirements.N is chosen to be an integer equals 2^k,where k is a positive integer.In the example shown here, N is taken to be 8, i.e., k is taken to be 3. Figure (2) shows the details of a memory bank (one of N), indicated as a module, to be repeated N times. Each module consists, as shown, of the memory of the module, as well as the necessary latches and other control logic.

III. LINE-STORE SETUP

Analogue video input is sampled at intervals set by the sampling frequency f_s.These samples are applied to the Analogue-to-Digital Converter (ADC),and converted into digital words. Each digital word is latched in order that it would be written into the appropriate location after the location address has been set. The latch is necessary because of the difference between sampling speed and memory access time.

The output bits of ADDRESS Counter are grouped into two parts. The first part contains the Least Significant Bits (3 bits in this case, for 8 banks), which will select one of N memory banks (8 in this case). Therefore, these bits are applied to an appropriate decoder/demultiplexer (3-to-8 lines, in this design), the outputs of which are connected to the Chip Select of corresponding memory chips. The second part comprises the remaining higher significant bits, (Most Significant Bits MSB),and will address a specific memory location in the selected module (bank). This means that, the first sample in a television line will be stored in the first location of the first bank, the second sample in the first location of the second bank, and so on, until the N^{th} sample will be stored in the first location of the N^{th} bank. The next sample, (N+1) is then stored in the second location of first bank, and so on the alternation proceeds as in the first vector of N samples, except that the words in this case will be written in the second location in each bank, respectively. Table (I) shows the layout of different samples (words) in the memory locations. It may be interesting to note that, although the second part of ADDRESS bits are slower in change, they also must be latched as well, in order that the appropriate address is selected for the corresponding location.

IV. MULTIPLEXING DEPTH

Depth of multiplexing is decided upon the relation between the access time of memory used,and the required sampling rate adequate for a particular application. For obvious reasons, related to the digital and binary circuitry, the number of multiplexing levels, (depth of multiplexing) is chosen to be

$N = 2^k$, where k is a positive integer.

Practical values of N = 4, 8, or 16 (i.e., k = 2, 3, or 4) are used. Assuming a low cost commercially

available memory, with access time of about 450 ns. (standard for MOS technology), and assuming a line-store to be compatible with existing analogue TV standards. Therefore,the total interval of an ordinary 625 line/frame, 25 frame/second TV line is 64 u sec. Number of samples/line is decided upon the facts of resolution and nature of image. But, again for compatibility with monochrome and colour TV standards, a sampling frequency is usually used in the range of $(2.5 - 3)f_{sub}$ [5-7], where f_{sub} is the chrominance subcarrier. In such cases, the frequency is in the range of 13 MHz.

i.e. 1 line → $13 \times 10^{6} \times 64 \times 10^{-6} = 850$ samples

A sampling rate faster than this,would be of a maximum sample number of 1024 (2^{10}, as mentioned before), in which the sampling interval should be

$$64 \text{ us.} / 1024 = 62.5 \text{ ns.}$$

therefore, depth of multiplexing would be :

$$N \geq 450 \text{ ns.} / 62.5 \text{ ns.} = 8$$

Using a depth of 16 will enable such a line-store to work efficiently, even with other special digital TV standards, in which both number of lines/frame, and samples/line are dictated by the requirements of the binary nature of digital electronics' world of today.

Table (II) shows sampling intervals for different values of samples/line, for the usual 64 usecond line, where Table (III) shows different possibilities of both lines/frame and samples/line, and corresponding time intervals in these cases.

Table (I). Samples locations in different memory banks of the television line-store.

Sample No. in line	Bank No.	Location in bank.
1	1	1
2	2	1
3	3	1
.	.	.
.	.	.
N	N	1
N+1	1	2
N+2	2	2
N+3	3	2
.	.	.
.	.	.
2N	N	2
2N+1	1	3
2N+2	2	3
.	.	.
3N	N	3
.	.	.
.	.	.
.	.	.
(M-1)N+1	1	M
(M-1)N+2	2	M
.	.	.
.	.	.
MN	N	M

Note: the Table shows the location of sample ordered:

$$(i - 1).\ N + j \quad , \text{ where}$$

i is the order of the vector, and varies from 1 to M

j is the order of the vector in a line, varying from 1 to N

N data vector size (number of data samples in a single vector),

M is the number of vectors in the TV line.

Table (II). Sampling intervals for different number of samples, for ordinary TV line.

No. of Samples per line.	Sampling interval in ns.
1024	62.5
512	125
256	250
128	500

Note: the simplicity apparent in values of intervals is due to the coincidence that the line period (64 us) is itself, an integer powered integer(2^6).

Table (III). Sampling intervals for different 'Binary Compatible' Television line standards.

Lines/frame	Samples/line	Sampling interval ns.
1024	1024	38.15
High resolusion	512	76.30
	256	152.6
512	1024	76.30
Medium resolusion	512	152.6
	256	305.2
256	1024	152.6
Low resolusion	512	305.2
	256	610.4

CONCLUSION

A television line-store is designed,using standard (normal speed, low cost) memory chips. The problem of the long access time of MOS memory is solved by using memory 'modules'. Different modules are addressed, in turn, using multiplexing technique.

The depth of multiplexing of 8 was found to be adequate for a variety of television standards. For a very high resolution 1024 line/frame, 1024 sample/line digital television system, the multiplexing should be of a depth of 16. In such case, the main designing procedures will remain the same, except for the decoding of the ADDRESS low significat bits.

REFERENCES

[1] Thorpe, P.L.M., "Contour Reduction for Digital Monochrome Image Signals", Ph.D.Thesis, University of Bradford, UK, 1979.

[2] Chambers,J.P.,"The Use of Digital Techniques in Television Waveform Generation",IBC 1974, IEE Conf. Publ. 119, pp.40-46, Sept. 1974.

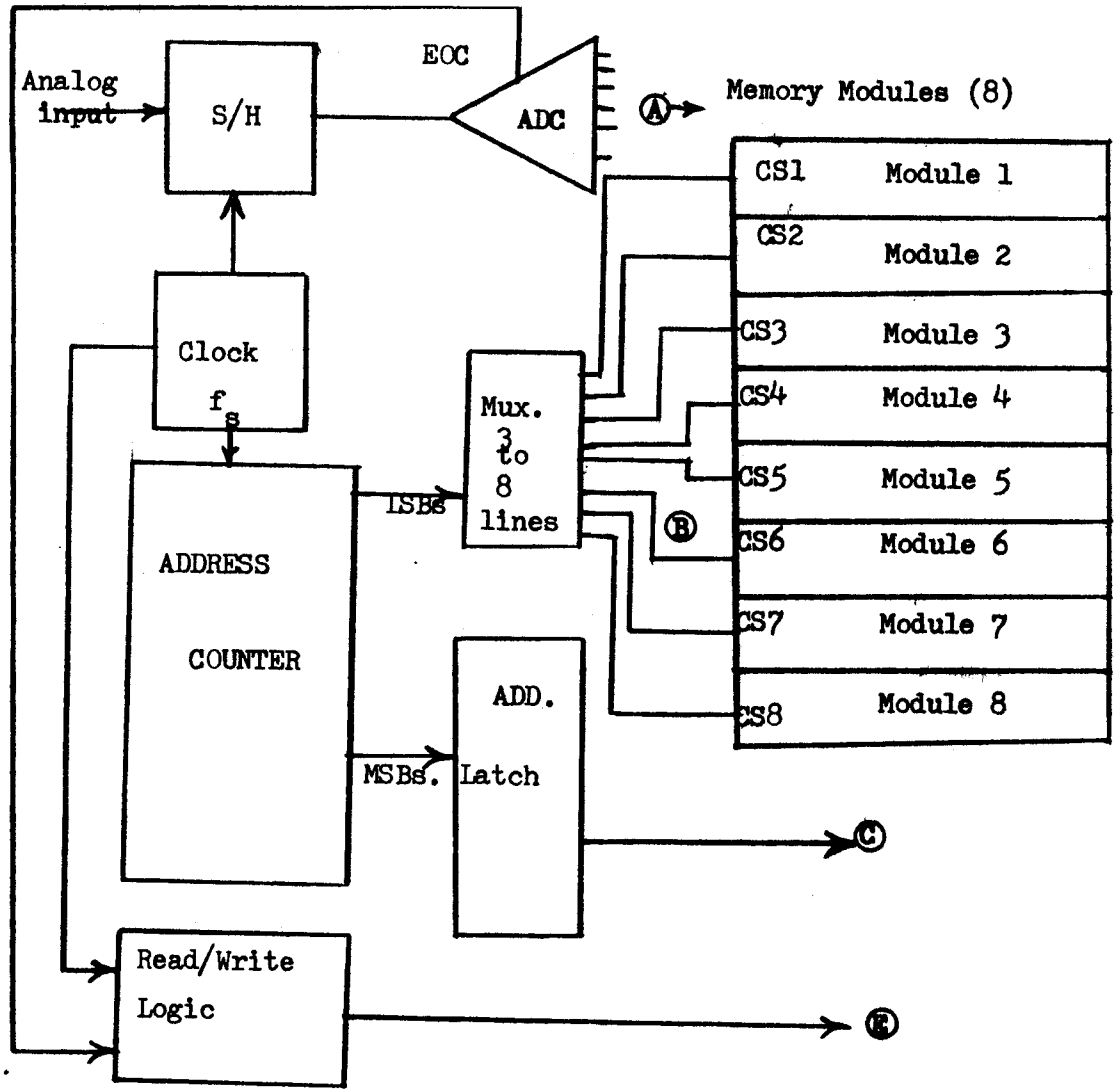
[3] Taub, H.,and Schilling, D., "Digital Integrated Electronics", McGraw-Hill Inc., 1977.

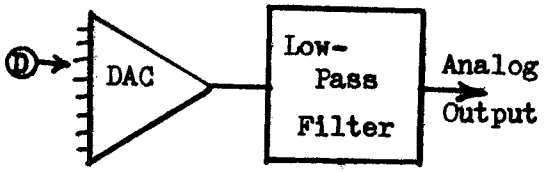
[4] Blood, Jr., W.R.,"MECL System Design Handbook", Motorola Semiconductor Products,Inc., Phoenix, Arizon, Oct. 1971.

[5] Downing,O.J.,and Gallagher, J.C., "A Feasibility Study of the Application of Digital Techniques to Television Studio Systems", Independet Television Companies Association Report 101/75, Sept.1975. London.

[6] Specification of television standards for 625-line system I transmissions., January 1971, BBC and ITA, London.

[7] Devereux, V.G., "Digital Video: differential coding of PAL signals based on differences between samples one subcarrier period apart", BBC Research Report BBC RD 1973/7, June 1973, London.





Figure(1). Block diagram of a TV line-store.

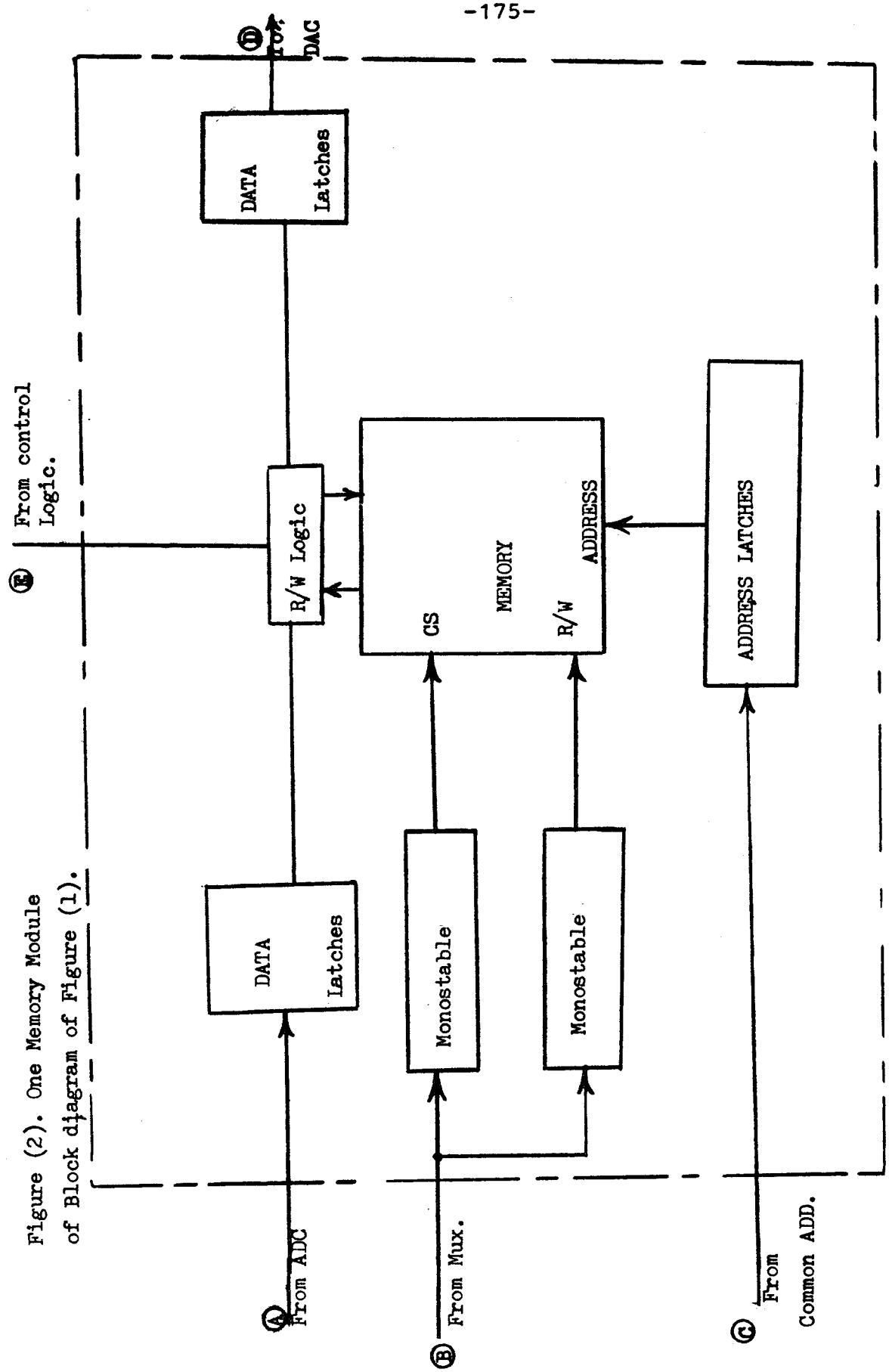


Figure (2). One Memory Module of Block diagram of Figure (1).