Mansoura University — Fourth Year Electronics
Faculty of Engineering — June 2012
Electronics&Comm. Dept. — Time: 3 hrs

Integrated Circuits Final Exam [Total : 100 marks]

Attempt All Questions

1-a) True Or False : each statement with T Or F.
- System-on-a chip: combine only some PLDs and FPGAs.
- CMOS domino is ratio circuit logic.
- Dynamic power dissipation increases linearly with frequency of operation.

b) Short Answers.
- The pitch of metal1 is equal to .....
- Changing beta ratio of CMOS inverter changes .....
- If the power supply voltage of a chip increases,the gate capacitance of each transistor will .....

c) Explain : - FPGA based on: its structure,programmability,and micro cell.
- Top-down and Bottom-up design,which is better ?

d) Prove that we usually implement the pull-up network with PMOS and pull-down network with NMOS.

2-a) Design programmable array logic has the inputs x,y,and z,and its outputs F1,F2,and F3. The outputs are given by :
$F1 = xy + x\bar{z}$, $F2 = x\bar{y} + x\bar{z}$, $F3 = xy + \bar{y}z$ .What are the types of its outputs ?

b) Explain CMOS transistor fabrication steps and define the types of package and its problems.

c) Calculate the noise margins of the DMD, with the parameters:
$V_{DD} = 3.3$ V $V_{TD} = 0.6$ V $V_{TU} = -0.8$ V knu =knd = 60 $\mu A/V^2$
(L/W)d =2 (L/W)u = 12

3-a) Prove that Vinv is an insensitive to Rinv in CMOS inverter.
Define its properties and noise in digital ICs.

b) Calculate the noise margins of a CMOS inverter with the following parameters:
NMOS $V_{TN} = 0.6$ V kn = 45 $\mu A/V^2$ (W/L)n = 8
PMOS $V_{TP} = -0.8$ V kp = 15 $\mu A/V^2$ (W/L)p = 12
Assuming $V_{DD} = 3.0$ V

4-a) Realize: XNOR Using CMOS gate in terms of PMOS and NMOS only .
Sketch its stick diagram.

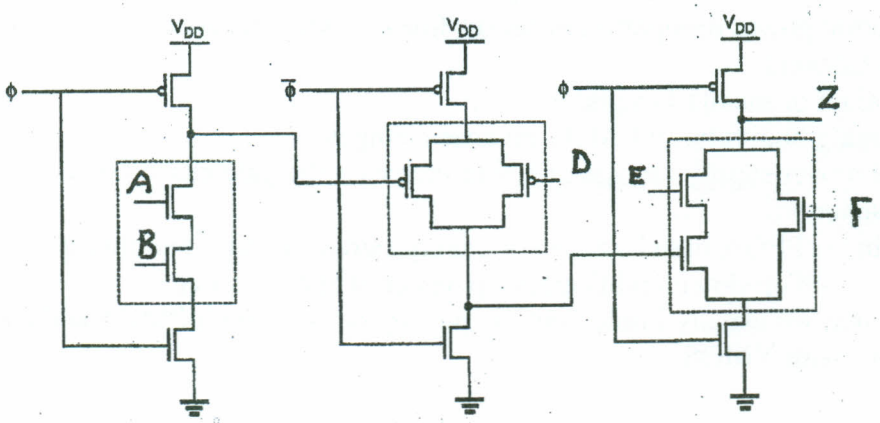
b) Explain NMOS dynamic shift register(DSR) using DMD and CMOS DSR using transmission gates (TGs). Define,which is better ?

c) Design 4:1 multiplexer using TGs.

5-a) Derive an expression for Pseudo NMOS inverter ratio and show that such Inverter is typical in CMOS VLSI .

b) Explain a recent BiCMOS inverter,why such circuit is faster than static one.

c) In the circuit back,explain NORA logic. Such NP logic has three stages .
Determine the logic function at output Z.


V_{DD}
V_{DD}
V_{DD}
ϕ
$\bar{\phi}$
ϕ
A
B
D
E
F
Z

Mansoura University	Fourth Year Electronics
Faculty of Engineering	June 2012
Electronics&Comm. Dept.	Time: 3 hrs

Integrated Circuits Final Exam [Total : 110 marks]

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c) Explain Domino CMOS logic.
Detrmine the output F = '((A + B) C + DE)' using Domino CMOS.