HARDWARE IMPLEMENTATION OF CONTINUOUSLY VARIABLE SLOPE ADAPTIVE DELTA MODULATOR

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خلاصة :-

نظام التشفير الدلتوى المتهايئ هو نظام اقتصادى لتشفير الاشارات الصوتية نظرا لسهولة بناء الدوائر الالكترونية الخاصة به وكذلك لأنه يحتاج الى وحدة معلومات واحدة لارسال الفرق بين كل عينه من اشارة الدخل والقيمة التقريبية المتوقعة لها . هذه القيمة التقريبية تتكون بتجميع (تكامل) مايسمى . بحجم الخطوة . وفي النظام الدلتوى المتهايئ يتغير حجم الخطوة حسب معدل التغير في الاشارة المراد تشفيرها . في هذا البحث تم تصميم وبناء نظام التشفير الدلتوى المتهايئ ذو معدل التغير المستمر . كذلك تم تصميم وبناء جميع الدوائر الالكترونية التي استخدمت في الدراسة العملية لكفاءة هذا النظام عند معدل معلومات بين ١٦٠٠٠ ـ ٣٢٠٠٠ نبضة / ث .

وقد أمكن الحصول على اشارات صوتية في المستقبل ذات جودة عالية من النظام المشار اليه عندما أرسلت المعلومات الرقمية بمعدل ٣٢٠٠٠ نبضة / ث على قناة اتصال معدل الاشارة الى الشوشرة بها يساوى ١٥ ديسبل أيضا أمكن الحصول على اشارات صوتية ذات جودة جيدة في المستقبل عندما أرسلت المعلومات الرقمية بمعدل ١٦٠٠٠ نبضة /ث على قناة اتصال معدل الاشارة الى الشوشرة بها يساوى ٢٠ ديسبل .

ونظرا لبساطة النظام المقدم في هذا البحث وسهولة بناء دوائره الالكترونية يمكن استخدامه في الاتصالات التليفونية المشفرة أو الاتصالات ذات السرية العالية مثل الاتصالات العسكرية .

ABSTRACT

Adaptive Delta Modulation (ADM) coding is an economical method of digitally encoding speech signals. It is a one-bit differential coding scheme which compares the source signal $x(t)$ to an approximate signal $\hat{x}(t)$ which is then increased or decreased by a predetermined step size. This step size is adapted in proportion to the recent average slew rate of the input signal. For a given average signal slope, there is an optimum step size which will result in the maximum signal-to-quantisation noise ratio $(SNR)_q$, and it is desirable to adapt accordingly.

In this paper, design and implementation of the continuously variable slope adaptive delta modulation (CVSD) are considered. To study the effects of channel errors and data encryption (scrambling) on the performance of the system, a channel simulator, noise generator, and encrypter/decrypter are also designed and constructed. Experiments showed that the system provides high quality speech reproduction at bit rates of 32 Kbps and 15dB SNR on transmission channel. Moreover, a good quality speech reproduction is obtained at 16 Kbps and 20dB SNR on transmission channel.

The system reported here may be suitable for secure military communication, in a half-duplex mode, over noise corrupted channels.

INTRODUCTION

An important member of the class of differential waveform coders is the one-bit or two-level differential pulse code modulation, known as delta modulation (DM) [1-7]. The property of one-bit codeword eliminates the need for word framing at the transmitter (Tr) and receiver (Rv), and makes DM systems very attractive for many classes of digital communication (e.g., military, power limited satellite, land mobile channels, ... etc.). The simplicity of DM also makes it an important method for digital speech storage.

In DM systems, the sampling rate is chosen to be many times the Nyquist rate for the input signal. The effect of a higher sampling rate is to increase the prediction gain by increasing neighbouring sample correlations. Therefore, the variance of the prediction error should be low, and a rather

crude quantiser (one-bit) can provide acceptable performance.

In its simplest form, DM [2] operates on the basis of approximating the input signal by a series of linear segments of constant slope. Such a coder is known as linear delta modulation (LDM) [1,3]. Fig. 1, shows a simple block diagram for this LDM system.

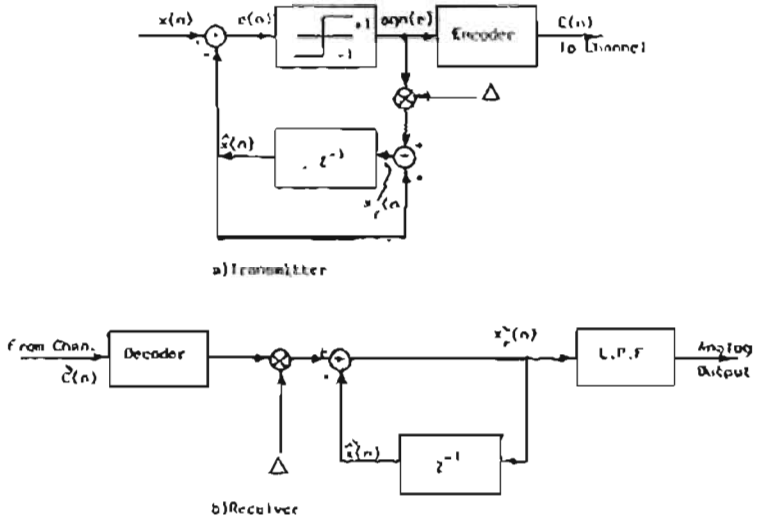


Fig. 1, Block Diagram of Linear Delta Modulation

It can be seen from Fig. 1(a), that the prediction error signal e(n) is given as

$$e(n) = x(n) - \hat{x}(n)$$

$$= x(n) - x_r(n-1) \qquad (1)$$

where $\hat{x}(n)$ is the predicted value of the input intelligence signal x(n), and $x_r(n)$ is the reconstructed signal. Note that, for noiseless channel $\hat{x}_r(n)=x_r(n)$, $\hat{x}'(n)=\hat{x}(n)$, and the codeword $c'(n)=c(n)$.

Let us define quantisation error as;

$$q(n) = x_r(n) - x(n) \qquad (2)$$

then, it can be shown that

$$e(n) = x(n) - x(n-1) - q(n-1) \qquad (3)$$

Thus except for the quantisation error q(n-1), e(n) is a digital approximation to the derivative of the input signal x(n). The reconstructed signal $x_r(n)$, can now be expressed as

$$x_r(n) = \Delta.\mathrm{sgn}(e(n)) + \hat{x}(n)$$

$$= \Delta.\mathrm{sgn}(e(n)) + x(n-1) + q(n-1) \qquad (4)$$

where Δ is a fixed step size. Again, except for the quantisation error, Eq.(4) is the digital equivalent of integration, in the sense that it represents the accumulation of positive and negative increments of magnitude Δ.

The principle of LDM operation is shown in Fig. 2. The sign of prediction error e(n) determines the direction of change in $x_r(n)$ by a step magnitude Δ. The reconstructed signal $\hat{x}_r(n)$ must be lowpass filtered to the original bandwidth to produce an approximation to x(n). Moreover, Fig. 2

shows two types of distortion caused by LDM. These are known as "slope overload" and "granular" distortions. The slope overload occurs when the step size is too small to follow a steep segment of the input signal. Granular noise occurs as a result of quantising the signal to a step size Δ; the larger Δ is made, the greater the granular noise. This noise becomes excessive when the step size is very large compared to the slope of the input signal. When the input is zero (idle channel condition), the output of LDM will be 0 1 0 1 0 1 ..., and as a result, the reconstructed signal will alternate about zero with a peak-to-peak variation of Δ.

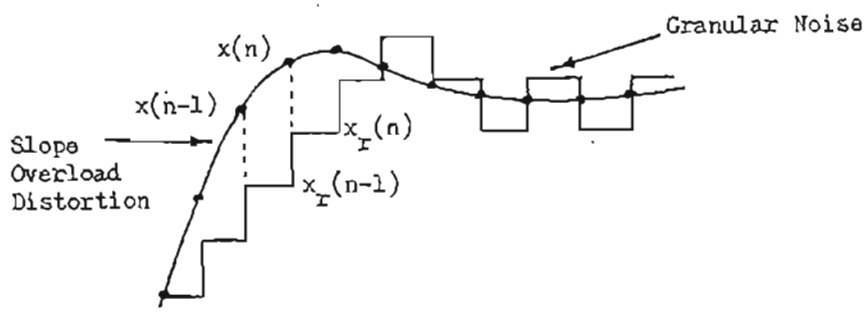


Fig. 2, Principle of LDM Operation

ADAPTIVE DELTA MODULATION

The performance of DM can be improved by using an adaptive quantiser. A wide variety of adaptive delta modulation (ADM) systems have been proposed in the literature [3,5,6,8]. Most step size updating schemes are of the feedback type in which the step size is adapted at both the transmitter and the receiver on the basis of the transmitted bit stream. The feedback adaptation method maintains the advantage that no synchronisation of bit patterns is required (for a noise free channels) since, the step size information can be derived from the codeword sequence $\{c(n)\}$ at both the transmitter and the receiver. The principle of operation and a general block diagram for ADM are shown in Figs. 3 and 4 respectively. In Fig. 3, it is shown that the variable step size $\Delta(n)$ increases during a steep segment of the input signal and decreases when the input is slowly varying. This requires a suitable rule for step size adaptation. In this section, we illustrate the use of ADM through the analysis of one specific adaptation algorithm. There are many other possibilities which can be found in the literature [1 - 9].

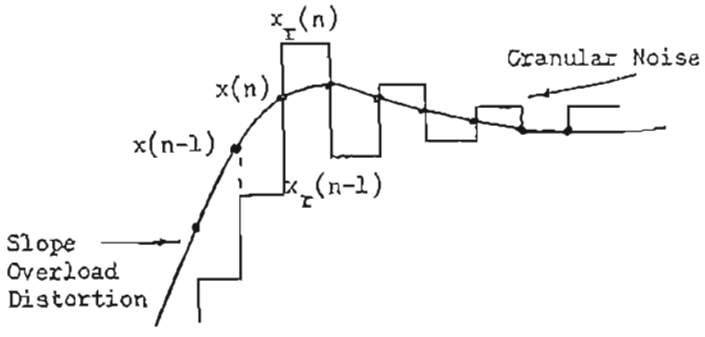


Fig. 3, Principle of Adaptive Delta Modulation Operation

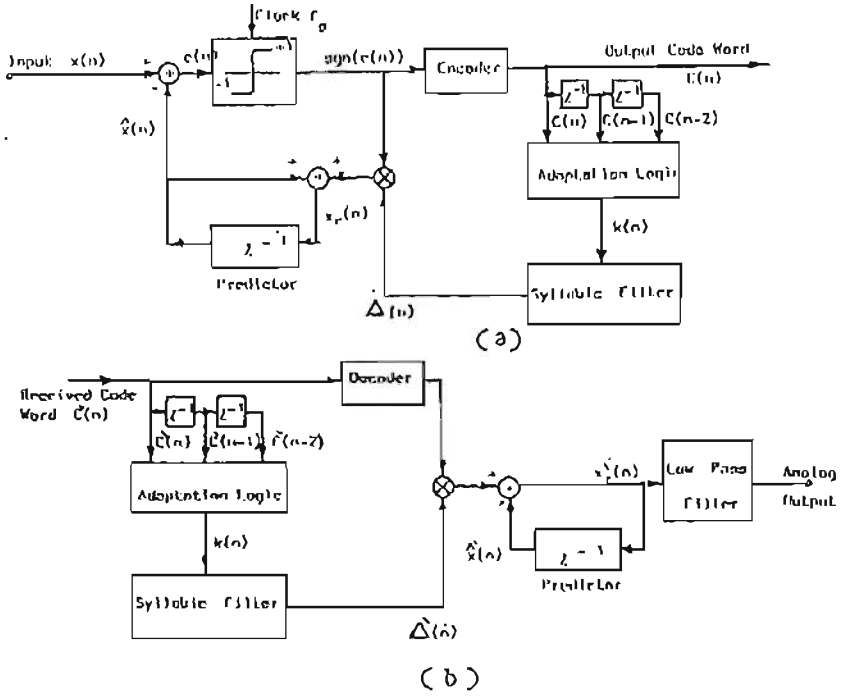


Fig. 4, Block Diagram for Continuously Variable Slope Adaptive Delta Modulation.
a)Transmitter b)Receiver

The system considered here, known as continuously variable slope delta modulation (CVSD) [6] is illustrated in Fig. 4. In this system the quantiser adjusts its step size $\Delta(n)$ based on the output bit sequence {c(n)}. When three consecutive bits of the same polarity are detected by the adaptation logic, the logic sets the control signal k(n) to one, and thus increases the step size $\Delta(n)$ toward the maximum step size Δ_{max}. Such conditions occur when the coder is slope-overloaded. But, for the input of nearly constant level or slowly varying signal, three or more consecutive like bits occur infrequently. When the adaptation logic does not detect the three consecutive like bits, then the logic sets k(n) to zero to decrease the step size $\Delta(n)$ toward the minimum step size Δ_{min}.

The step size adaptation is controlled by a time constant $1/\alpha$ (called the syllabic time constant) which is of the order of several milliseconds. The syllabic adaptive DM algorithm adjusts the magnitude of build-up and decay of $\Delta(n)$ at a much slower rate compared with instantaneous variations in speech signal. Syllabic adaptation is suitable for applications requiring low sensitivity to channel errors with speech quality requirements below those required for commercial communication channels.

In Fig. 4, the prediction of the input signal is performed through the delay Z^{-1} and the step size adaptation rule given in [10] as

$$\Delta(n)=\text{Exp}(-\alpha T).\Delta(n-1) + G(1-\text{Exp}(-\alpha T)); \text{ If } c(n)=c(n-1)=c(n-2) \quad (5\text{-a})$$

and

$$\Delta(n)=\text{Exp}(-\alpha T).\Delta(n-1) \quad ; \quad \text{otherwise} \quad (5\text{-b})$$

where T is the sampling interval, G is the step size increase factor, and

$$\Delta_{min} < \Delta(n) < \Delta_{max}$$

HARDWARE IMPLEMENTATION

1-CVSD Implementation

There is a variety of IC CVSD encoders and decoders in today's semiconductor market. When both encoder and decoder are packaged in the same IC, it is called an enCOder/DECoder, or CODEC. The CODEC IC used in this work is the MC3417 from MOTOROLA (See Appendix A for pin connections and internal structure). This IC operates in the half-duplex mode, i.e., data can be transmitted and received, but not at the same time. Based on this specifications, the system reported here is constructed as two remote stations each of them operates as a half-duplex encoder/decoder. That is, each station consists of only one chip MC3417 and operates as a half-duplex transmitter/receiver.

Fig. 5, illustrates a block diagram for the MC3417 CVSD chip. It can be seen from this figure that each chip consists of two separate parts, the encoder and the decoder. The encoder consists of a digital sampler and estimate filter (integrator). In addition, the encoder consists of an algorithm logic circuit, filter, and pulse amplitude modulator. The digital sampler and the estimate filter perform the LDM process shown in Fig. 1. The algorithm logic circuit, the filter, and the pulse amplitude modulator monitor and detect the amplitude change of the input intelligence signal and adapt the output of the integrator to the amplitude change by modulating the digital signal.

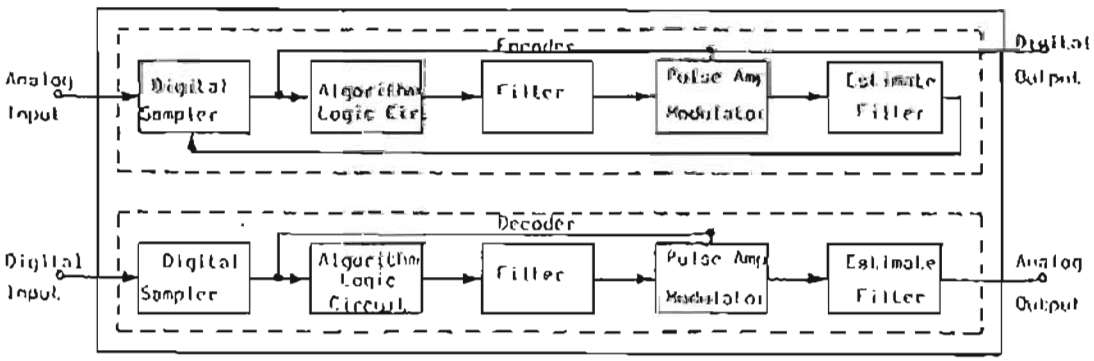


Fig. 5, Block Diagram For MC3417 CVSD Chip.

In Fig. 6(a & b), abrupt changes in the intelligence signal are shown in the digital signal by long sequences of logic 1's or logic 0's, while non-abrupt changes include alternating logic 1's or logic 0's. The algorithm logic circuit detects abrupt amplitude changes of the intelligence signal by comparing three consecutive pulses of the digital signal. When three pulses of the digital signal match it is considered an abrupt amplitude change, and a pulse signal is output by the algorithm logic circuit (Fig.6-c). The filter acts as an integrator, integrating the pulses from the algorithm logic circuit into ramp signals as shown in Fig. 7(a). The filter outputs the ramp signal (control signal) to the pulse amplitude modulator. The pulse amplitude modulator receives both the control signal and the digital signal as shown in Fig. 7(b). The pulse amplitude modulator uses the control signal to modulate the amplitude of the digital signal. The modulated digital signal is used as input to the estimate filter. The estimate filter integrates the modulated digital signal, and outputs a ramp signal as shown in Fig. 7(c). From Fig. 7(c), it can be seen that the integrated signal is increased to match the change in amplitude of the input intelligence signal in Fig. 6(a).

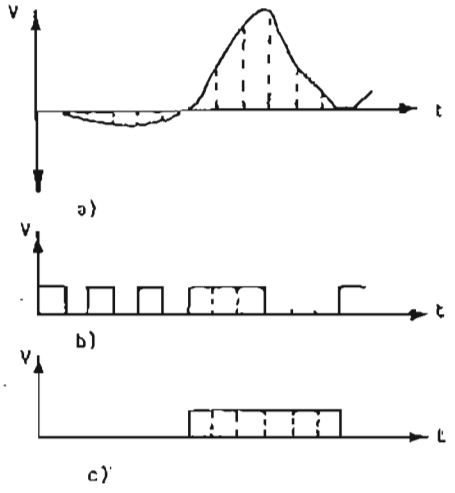


Fig. 6,a)Intelligence Signal b)Digital Signal
c)Pulse Output From Algorithm Logic Circuit.

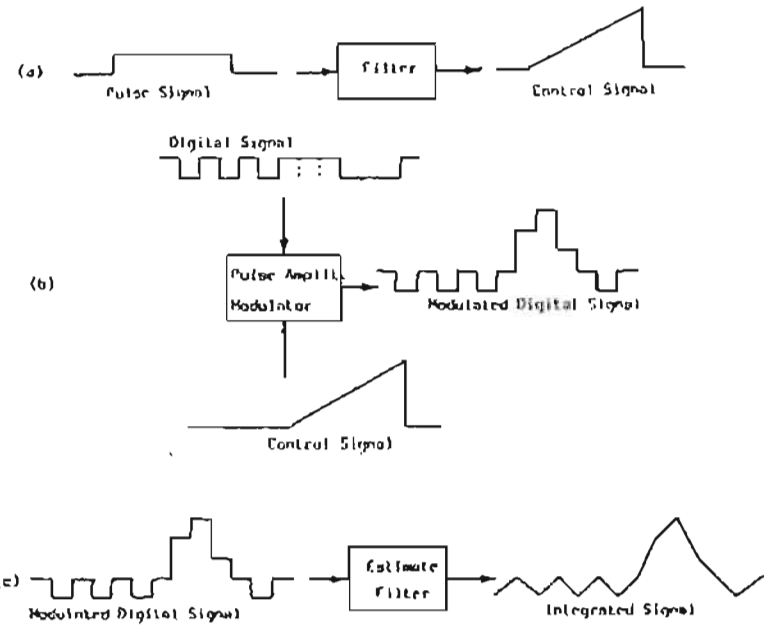


Fig. 7, a)Filter Function b)Pulse Amplitude Modulator Function
c)Estimate Filter Function

The encoding operation of the CODEC is illustrated in Fig. 8. In this figure the intelligence signal drives the non-inverting input of the comparator while the feedback signal drives the inverting input. During each Tr. clock, the comparator compares the present voltage of the intelligence signal with the feedback signal. The comparator outputs a logic 1 or logic 0 to the D-type flip flop, depending on the voltage levels of the intelligence and feedback signals. The D-type flip flop outputs the logic 1 or logic 0 as a pulse at Q. This is the digital signal transmitted to the receiver (decoder). In the same time, the digital signal is input to both the algorithm logic circuit and the pulse amplitude modulator. The algorithm logic circuit outputs a pulse signal to the filter, and the filter integrates the pulse signal into a control signal. The control signal is input to the pulse amplitude modulator, where it is used to modulate the digital signal.

The modulated digital signal is integrated into the feedback signal by the estimate filter and input to the comparator.

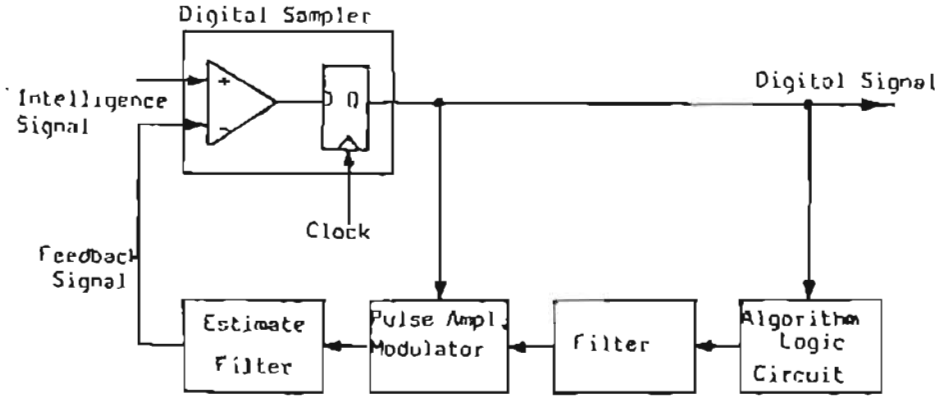


Fig. 8, CVSD Encoder Block Diagram.

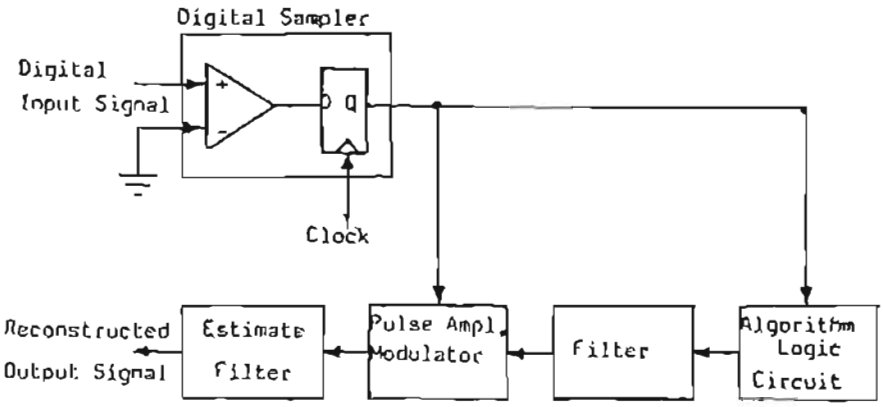


Fig. 9, CVSD Decoder Block Diagram.

The decoder of the MC3417 consists of a digital sampler and an estimate filter (integrator). In addition, it also consists of an algorithm logic circuit, a filter, and a pulse amplitude modulator (see Fig. 5). The decoding operation of the CODEC, shown in Fig. 9, may be explained as follows. The digital signal drives the non-inverting input of the comparator while the inverting input is connected to ground. This causes the comparator to act as a buffer, with the digital signal input to the D-type flip flop from the comparator on each Rx. clock signal. The digital signal is output by the D-type flip flop to both the algorithm logic circuit and the pulse amplitude modulator. The algorithm logic circuit output a pulse signal to the filter where it is integrated into a control signal. The control signal is input to the pulse amplitude modulator, where it is used to modulate the digital signal. The modulated digital signal is integrated by the estimate

filter and output as the reconstructed intelligence signal. Note that the Rv. clock signal used by the decoder must be exactly of the same frequency as the Tr. clock signal to accurately reconstruct the intelligence signal.

Two circuits identical to that illustrated in Fig. 10, were designed and constructed. Switch S_1 (normally open switch) connects pin 15 to $+V_{cc}$ volt (Logic High) or zero volt (Logic Low) for either encode or decode operation respectively. Switch S_3 (two-way switch) supplies either the digital data from channel (receive mode) to the decoder or the digital data output from the encoder (transmit mode) to the channel. Switch S_2 disconnects the analog output during transmission mode. The three switches should be ganged together so that their settings may be changed by only one touch. Capacitor C_1 (0.1 UF,12 V.) provides a.c. coupling. Resistors R_2, R_3, R_4, and the reference voltage at pin 10 bias the Op Amp inputs to half the supply voltage for unipolar (single polarity) operation. Resistor R_5 and capacitor C_3 set the time constant of the estimate filter to $10\times10^{3}\times0.1\times10^{-6}$ = 1 m.sec. Resistor R_7 and capacitor C_4 set the time constant of the syllabic filter to $60\times10^{3}\times0.1\times10^{-6}$ = 6 m.sec. (typical time constant values of 6 to 50 m.sec are used in speech coding). Resistor R_8 is a pull-up resistor for the open collector coincidence output. This output will be low whenever the content of the internal shift register is all ones or all zeros. Resistor R_6 adjusts the loop gain of the CODEC and must be no larger than 5 KΩ to maintain stability.

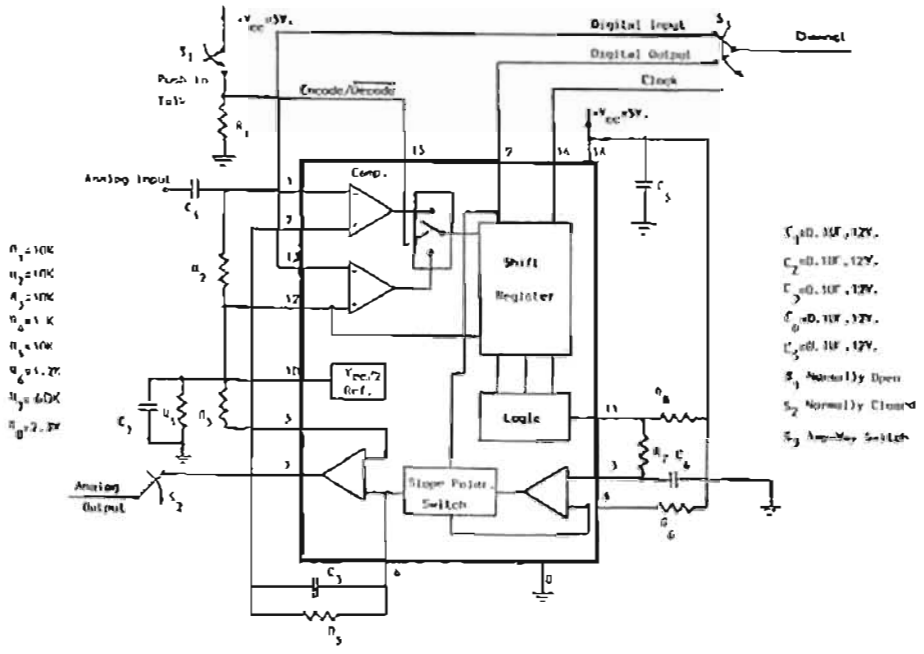


Fig. 10, Adaptive Delta Modulation CODEC

2-Channel Simulator

The channel simulator designed and constructed is shown in Fig. 11. It consists of a first order lowpass filter and summing amplifier. The lowpass filter operates at unity gain and its cut-off frequency can be selected using the bandwidth select switch S_4. The bandwidth in each case is given as

$$f = 1/(2\pi RC_i) \quad ; \qquad i=1,2,3,4 \qquad (6)$$

The transmitted signal is applied to the lowpass filter input. The output of the lowpass filter is added to a white noise signal at the unity gain summing amplifier. A SNR settings of 20dB, 15dB, 10dB, and 5dB can be selected using S_5.

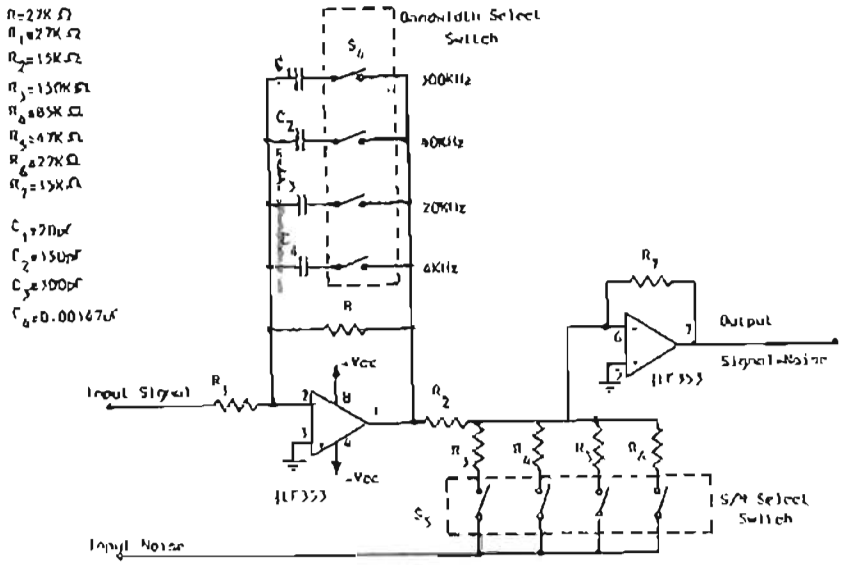


Fig. 11, Channel Simulator Circuit

3-Noise Generator

White, or thermal, noise is the background hiss heard in radio signals and telephone conversations. It is generated by the random movement of electrons in a resistor or semiconductor device. In this work, white noise is simulated by a pseudonoise (PN) sequence with a very long length.

Pseudonoise sequence [11] may be generated using the linear feedback shift register shown in Fig. 12. It is made up of a 3-stage register, a modulo-2 adder, and a feedback path from the adder to the input of the register. The shift register operation is controlled by a sequence of clock pulses (not shown). At each clock pulse the contents of each stage in the register is shifted one stage to the right. Also, at each clock pulse the contents of stages X_2 and X_3 are modulo-2 added, and the result is fed back to stage 1. The PN sequence is defined to be the output of the last stage (X_3). The length of the PN sequence is defined by

$$P = 2^n - 1 \qquad (7)$$

where n is the number of stages in the shift register. If stage X_1 is initially filled with a one and the remaining stages are filled with zeros, i.e., the initial state of the register is 100, then it can easily be shown that the succession of register states will be as follows: 100, 010, 101, 110, 111, 011, 001, 100. Since the last state corresponds to the initial state, then the register repeats the foregoing sequence after 7 clock pulses ($2^3 - 1 = 7$). The output sequence from X_3 is 0010111.

A circuit diagram for the constructed white noise source is shown in Fig. 13. It consists of three parts, PN sequence generator, lowpass filter, and buffer amplifier. The PN sequence is generated by the chip HM5837 which consists of a clock generator and a seventeen stage linear shift register.

This generator outputs a random sequence pulses that repeats itself after $2^{17} - 1$ clock pulses. White noise is generated by lowpass filtering of the random sequence obtained from HM5837. A second order infinite gain multiple feedback lowpass filter consists of half LF353, R_2, R_3, C_2, and C_3 is used for this operation. The cut off frequency for this filter configuration is given by

$$f_c = 1/(2\pi \sqrt{R_2 R_3 C_2 C_3}) \qquad (8)$$

The white noise is buffered by the buffer amplifier circuit consisting of the second half of LF353.

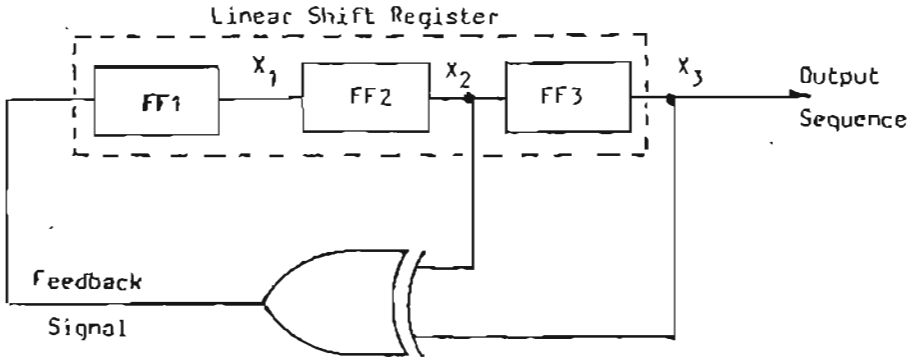


Fig. 12, Simplified Block Diagram of PN Sequence Generator.

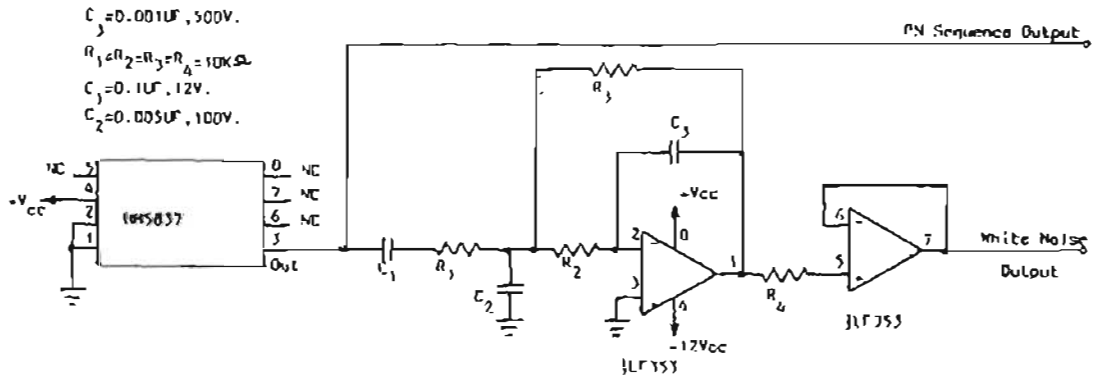


Fig. 13, Circuit Diagram for White Noise Source.

An experimental sample of the outputs from the circuit shown in Fig.13 is illustrated in Fig. 14. Fig. 14(a), shows the output from the PN sequence generator and Fig 14(b) shows the corresponding output from the L.P.F., which can be considered as a random sine wave signal.

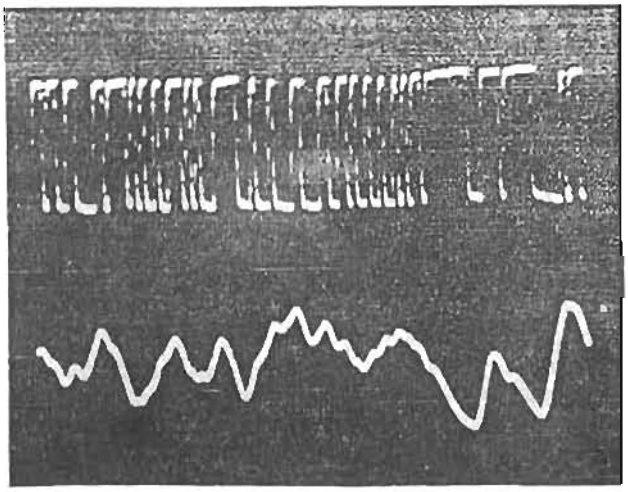


Fig. 14, Output From The Noise Source

4-Bit Error Counter

One way to determine the effect of noise on the transmitted signal is to measure the bit error rate (BER). The BER is the ratio of the number of incorrect bits received during transmission to the number of bits transmitted. Therefore, the BER is determined by counting the number of bit errors over a period of time, then the number of bits transmitted is determined by multiplying the data rate of the transmission by the time period of the count. Finally, the number of bits in errors is divided by the number of bits transmitted, i.e., BER = E/T R, where E is the number of bits in error, T is the time period of count, and R is the data rate.

The circuit designed and constructed to count the number of bit errors is shown in Fig. 15. It consists of a bit error counter and 15 sec. timer.

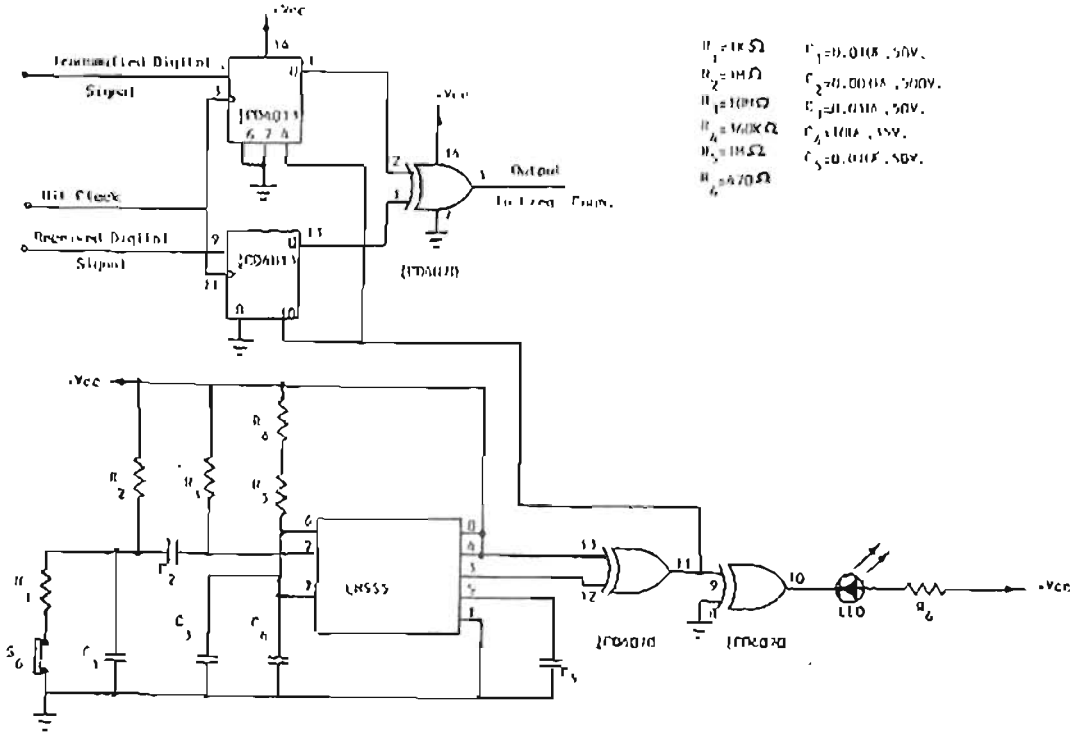


Fig. 15, Bit Error Counter and 15 sec. Timer.

a)Bit Error Counter: It consists of the chip CD4013 dual D-type flip flop. The clock inputs of both flip flops are tied together and connected to the bit clock of the system. The Set inputs of both flip flops are connected to low logic level. The output of the timer is XORed with high logic level and the output of the XOR gate CD4070 is connected to both Reset inputs of the flip flops. Therefore, during the 15 sec. pulse from the timer, both Set and Reset inputs will be low, and the outputs of the flip flops depend on the D inputs and the clock. The D input of the first flip flop is connected to the transmitted data while the D input of the second flip flop is connected to the received data. The Q outputs of both flip flops are XORed together to form the final output. A pulse is generated at the output of the XOR each time the data do not match (error occurs).
b)The 15 sec. Timer: It is based on the chip LM555 connected as monostable generator. When a negative trigger signal is applied to pin 2 through switch S_6, a high output pulse will appear at pin 3. The duration of this pulse is controlled by R_4, R_5, C_3 and C_4 shown in Fig. 15 as;

$$\text{Pulse Duration} \approx 1.1\ R\ C \qquad (10)$$

where $R = R_4 + R_5$, and $C = C_3 // C_4$. For a matter of convenience, a LED is connected in the timer circuit (lights during the 15 sec. pulse) to indicate the error counting time.

4-Encryter/Decrypter

Encryption, or scrambling is the process of changing the digital signal before it is transmitted. Decryption, or unscrambling, is the process of changing the encrypted digital signal to the original signal after reception. The encryption/decryption circuit used in this work is illustrated in Fig. 16. It consists of an XOR gate at both the encrypter and decrypter circuit and a synchronous random sequence (PN) signal applied to both. The PN sequence signal is taken from the PN noise generator of Fig. 13. At the transmitter, the digital signal (Fig.16-b) and the PN sequence signal (Fig.16-c) are input to an XOR gate. The output of the XOR gate (Fig. 16-d) is the encrypted signal. The encrypted signal is transmitted to the receiving station's decrypter. The encrypted signal (Fig. 16-d) and the PN sequence signal (Fig. 16-e) are input to an XOR gate. The output of the XOR gate is the decrypted digital signal (Fig. 16-f). Decrypting can only be done successfully if the PN sequence signal to the decrypter is an exact and synchronous replica of the PN sequence signal to the encrypter.

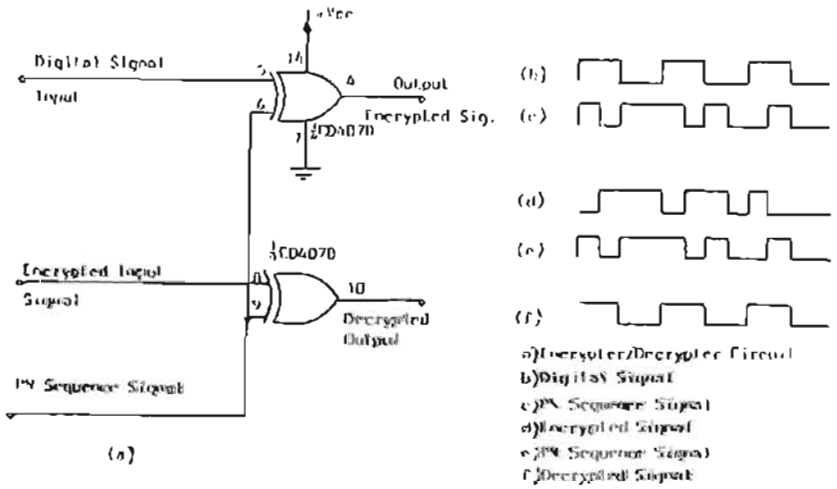


Fig. 16, Encrypter/Decrypter Circuit & Waveforms.

Experimental samples of the inputs and outputs to the encrypter/decrypter circuit are shown in Fig. 17. Fig. 17(a) shows the digital data input to the encrypter and Fig. 17(b) shows the corresponding encrypted digital data. Fig. 17(c) shows the digital data input to the encrypter at the transmitter and Fig. 17(d) shows the corresponding output from the decrypter at the receiver. It can be seen from Fig. 17(c) and Fig. 17(d) that the decrypter at the receiver provides an identical signal to the original signal input to the encrypter at the transmitter.

It is important to note that encryption/decryption process is mainly used for secure data transmission. This is due to the difficulty that an unauthorised listener would face in generating a synchronised replica of the PN sequence signal.

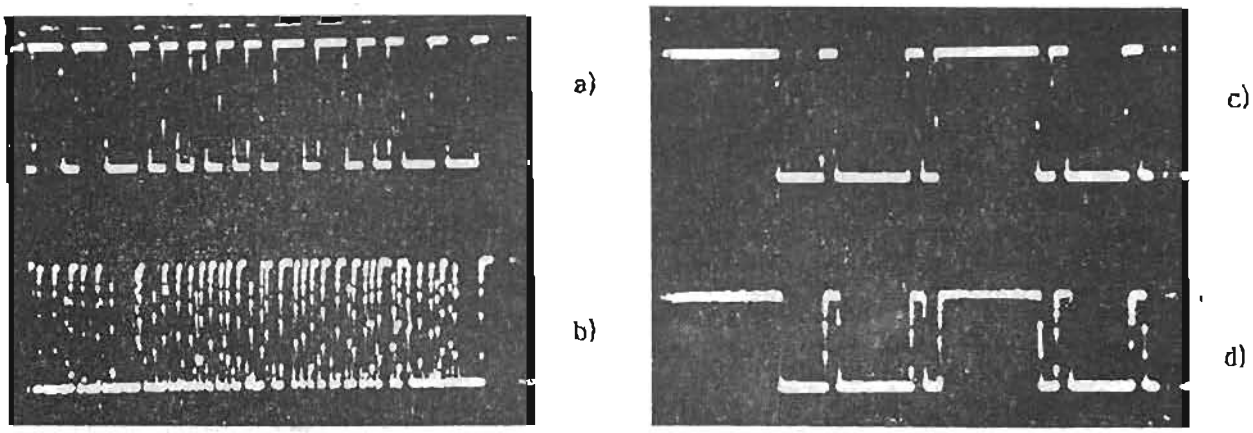


Fig. 17, Experimental Results From Encrypter/Decrypter Circuit.
a)Digital Data Input to the Encrypter.
b)Digital Data Output from the Encrypter.
c)Digital Data Input to the Encrypter.
d)Digital Data Output from the Decrypter.

EXPERIMENTAL RESULTS

A series of experiments were conducted to study the performance of the continuously variable slope adaptive delta modulation (CVSD) system presented in the previous section. The first part of these experiments was intended to show the ideal operation of the system, whereas the second part of the experiments was devoted to show the nonideal operation, i.e., effects of channel bandlimiting, additive noise, and encryption/decryption. In all experiments, the reconstructed signal from the CVSD receiver was passed to a programmable lowpass filter, an audio power amplifier, and a loudspeaker for listening tests.

Fig. 18(a) shows an 800Hz, 2Vp-p sine wave signal which was applied to the CVSD transmitter. Fig. 18(b) shows the corresponding digital data transmitted at 32Kbps to the receiver. Fig. 19(a) shows the reconstructed output from the CVSD receiver, and Fig. 19(b) shows the reconstructed signal after lowpass filtering with 2KHz L.P.F. Comparing Fig. 19(b) with Fig. 18(a), it can be seen that the received signal is identical to the original input signal.

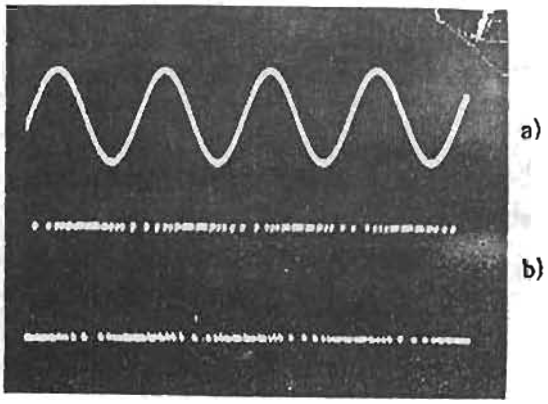


Fig. 18, a)Analog Input Signal
b)Digital Signal.

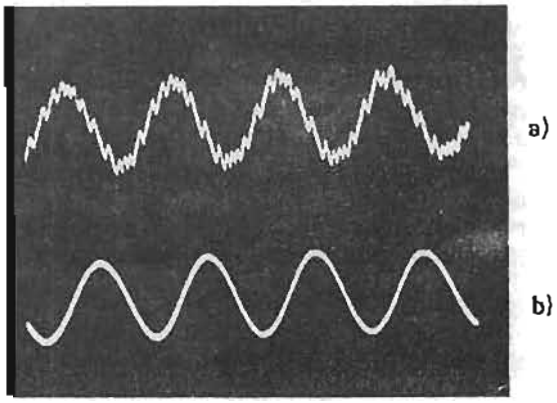


Fig. 19, a)Received Signal Before LPF
b)Received Signal After LPF.

Fig. 20(a) shows the original speech signal for a part of the word (آلو) bandlimited to 3.2KHz. This signal was applied to the CVSD transmitter and coded at a bit rate of 32Kbps (32KHz clock). Fig. 20(b) shows the corresponding received signal after lowpass filtering with a 3.2KHz L.P.F. Fig. 21(a) shows the original speech signal for a part of the word (آلو) bandlimited to 3.2KHz. This signal was transmitted at a bit rate of 16Kbps (the CVSD clock was changed to 16KHz). The corresponding received signal after lowpass filtering with 3.2KHz L.P.F. is shown in Fig. 21(b). The received speech in the above experiments, in general, was judged to be intelligible and of high quality. However, the listeners (Laboratories' Engineers and Technicians) judged the quality from the 32Kbps case as that obtained from the normal telephone system (analog telephone system). On the other hand, they showed some objections on the speech from the 16Kbps case due to the effect of quantisation noise heared in the background. This is an anticipated result, since the quantisation noise in DM system is inversely proportional to the cube of the sampling frequency (clock rate).

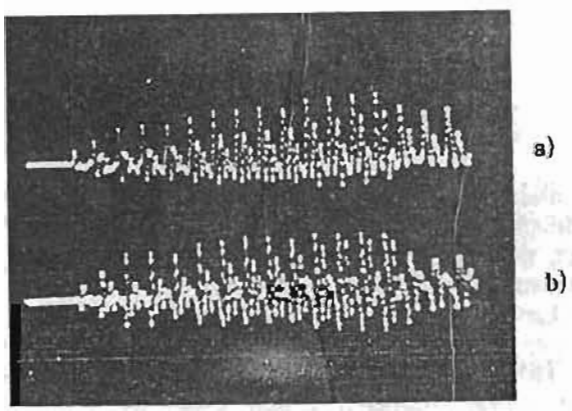


Fig. 20, a)Original Speech
Transmitted at 32Kbps.
b)Received Speech Signal

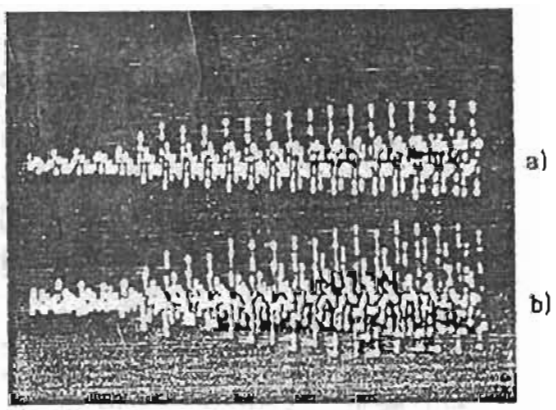


Fig.21, a)Original Speech
Transmitted at 16Kbps.
b)Received Speech Signal.

As shown in the above experiments, quantisation noise affects the digital signal of the CVSD system, but not to the point of destroying the reconstructed signal. When the received signal was passed through the loudspeaker, the quantisation noise can be heard but with little or no effect on the received signal. White noise also affects the digital signal of the CVSD system. The received signal will not be affected unless the SNR on the transmission channel is low.

In the following experiments, the speech signal was applied to the CVSD transmitter where it is converted to a digital signal. The digital signal was transmitted to the channel simulator circuit (Fig. 11) and combined with the white noise signal from the noise source circuit (Fig. 13). The combined signal was sent to the CVSD receiver, lowpass filter, amplifier, and loudspeaker. The results are shown in Table 1, Fig. 22, Fig. 23, Fig. 24, Fig. 25, and Fig. 26.

Table 1, BER Versus SNR on Transmission Channel for the CVSD System at Bit Rates of 32Kbps and 16Kbps Respectively.

Channel Bandwidth	20 KHz							
Bit Rate (Kbps)	32				16			
SNR (dB)	20	15	10	5	20	15	10	5
BER	0	0	0.011	0.091	0	0.005	0.026	0.103

Fig. 22(a) shows the digital data (at bit rate of 32Kbps) transmitted to the channel and Fig. 22(b) shows the received digital data from the channel with SNR of 10dB. Fig. 23(a) shows the digital data (at bit rate of 16Kbps) transmitted to the channel and Fig. 23(b) shows the corresponding received data from the channel with SNR of 15dB. Fig. 24(a) shows the original speech signal bandlimited to 3.2KHz (part of the word الو) which was transmitted at a bit rate of 32Kbps with a SNR = 10dB on the transmission channel. Fig. 24(b) shows the corresponding received signal after lowpass filtering with 3.2KHz L.P.F. Fig. 25(a) shows the original speech signal (bandlimited to 3.2KHz) which was transmitted at a bit rate of 16Kbps with a SNR = 15dB on the transmission channel. Fig. 25(b) shows the corresponding received signal after lowpass filtering to the original bandwidth. Fig. 26(a) shows the original speech signal (bandlimited to 3.2KHz) which was transmitted at a bit rate of 32Kbps with a SNR = 15dB on the transmission channel. Fig. 26(b) shows the corresponding received signal after lowpass filtering to the original bandwidth.

From Table 1 and Figs. 22 through 26, it can be seen that:

1-As the SNR on the transmission channel decreases, the BER increases.
2-The increase in BER is more pronounced in the 16Kbps case than in the 32Kbps case for the same SNR on transmission channel.
3-The distortion seen in the received signals illustrated in Figs. 24(b) and 25(b) is due to channel errors occured from the added white noise.
4-The received speech from the CVSD system at a bit rate of 32Kbps and a SNR= 15 dB on the transmission channel is identical to the original transmitted speech signal (see Fig. 26). This result was confirmed by the listeners.

The immediate conclusion which can be drawn here is that, the 32Kbps CVSD system requires no more than 15dB SNR on the transmission channel to provide a speech quality identical to that obtained in ideal operation. On the other hand, the 16Kbps CVSD system requires about 20dB SNR on the transmission channel to provide a speech quality identical to that obtained from the same system in ideal operation.

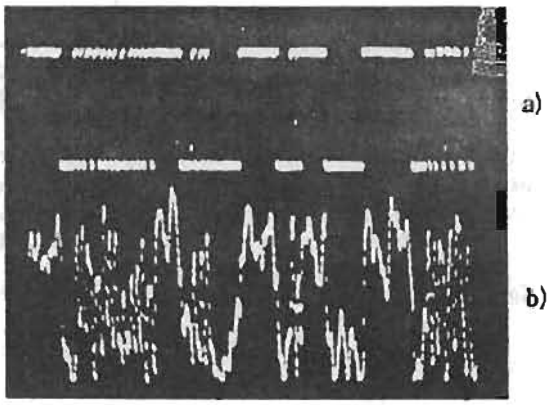


Fig.22, a)Digital Data to Channel.
b)Digital Data from Channel
With SNR = 10dB.

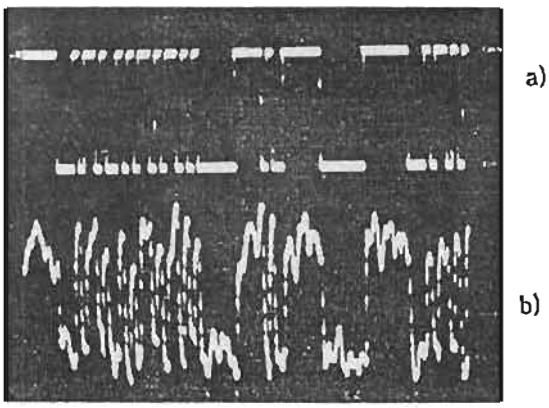


Fig.23, a)Input Data to Channel.
b)Digital Data from Channel
With SNR = 15dB.

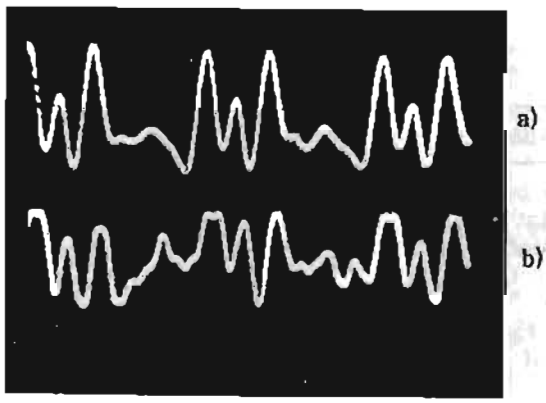


Fig. 24 a)Original Speech Signal
b)Received Signal from 32Kbps
System & SNR=10dB

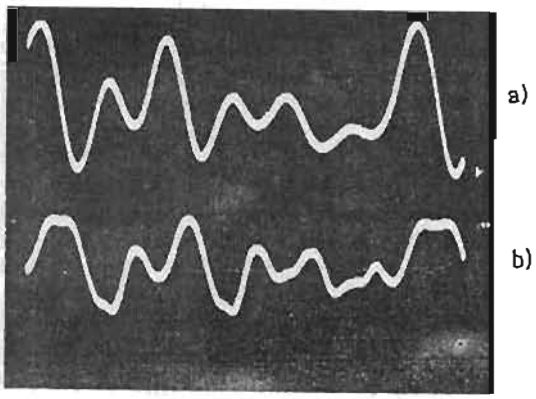


Fig. 25,a)Original Speech Signal
b)Received Signal from 16Kbps
System & SNR=15dB.

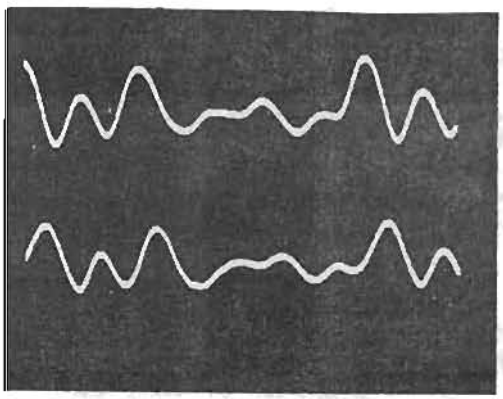


Fig. 26, a)Original Speech Signal Bandlimited to 3.2KHz. b)Received Signal from 32Kbps System & SNR=15dB.

Experiments similar to those conducted above were carried out to study the performance of the CVSD system with data encryption. The results obtained in the case of ideal operation (no restrections on channel bandwidth) were similar to those obtained without data encryption. However, for nonideal operation, a channel bandwidth almost twice as much as that used in the above experiments was required to retain identical results to those illustrated in Table 1 and Figs. 22 through 26. This result is anticipated, since data encryption spreads the signal bandwidth, i.e., increases the data rate on the transmission channel (see Fig. 17).

CONCLUSIONS

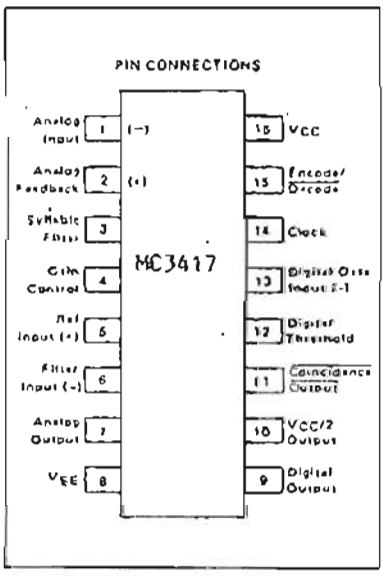
The continuously variable slope (CVSD) adaptive delta modulation system at two specific bit rates (32Kbps and 16Kbps) has been designed and implemented using the MC3417 chip from MOTOROLA. All other circuits (channel simulator, bit error rate counter, white noise source, and encrypter/decrypter) required for the experimental performance study were designed and constructed.

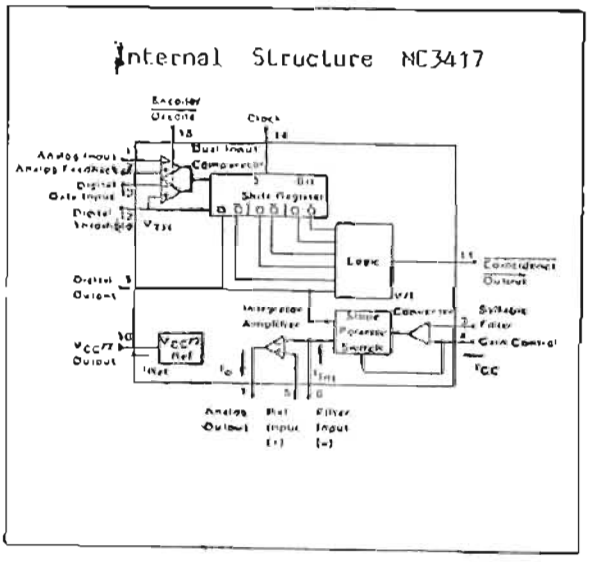
A high quality speech reproduction was obtained at the bit rate of 32Kbps using noise corrupted transmission channel with no more than 15dB SNR. Despite the effect of quantisation noise heard in the background, the system provided intelligible and good quality reconstructed speech at the bit rate of 16Kbps using noisy transmission channel with 20dB SNR.

The system was found to be insensitive to data encryption, i.e., it provided similar performance to that obtained without data encryption. However, the required transmission channel bandwidth was increased due to the increase in the data bandwidth. This is the price to be paid for more secure data transmission.

The 32Kbps system may find its applications in commercial telephone systems whereas, the 16Kbps system with data encryption may be suitable for secure military communications, in a half duplex mode, over noisy channels.

APPENDIX A





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